IN THE CLAIMS

Claims 35, 36, 42, 47,, 49, 51, and 55 – 57 have been cancelled. Claims 31, 39 – 41, 43, 46, 48, 50, and 52 – 54 have been amended, as follows:

Claims 1 – 30 (cancelled).

31. (currently amended) A system to manage energy usage of a processor, comprising:

a data communication network;

a transmitter, coupled to the data communication network, to invoke a protocol state machine to send a packet and to wait for an acknowledgment of receipt;

a receiver, in communication with the transmitter coupled to the data communication network, to receive, process, and verify the packet and to send the acknowledgment of receipt of the packet;

an incoming packet buffer, coupled to the protocol state machine in the transmitter, to store an incoming packet to be transmitted by the transmitter; and

a processor, coupled to the protocol state machine in the transmitter, the processor enters a low power, low clock rate mode while waiting for the acknowledgment of receipt of the packet from the receiver,

wherein the protocol state machine manages a power level of the processor based on a utilized capacity of the buffer and the transmitter awakens when the incoming packet buffer reaches a low water mark.

32. (previously presented) The system of claim 31, wherein the data communication network includes at least one of the Internet and an Intranet.

33. (previously presented) The system of claim 31, wherein the processor in the transmitter begins in a high power, high clock rate mode.

34. (previously presented) The system of claim 31, wherein the transmitter performs tasks to create packets for transmission, the tasks including at least one of dividing data into packets, adding protocol headers, or computing checksums.

Claims 35 and 36 (cancelled).

37. (previously presented) The system of claim 31, wherein the receiver includes an application buffer and after the receiver receives the packet, the packet is stored in the application buffer.

38. (previously presented) The system of claim 37, wherein the receiver includes a receiver protocol state machine and a receiver processor, and the receiver protocol state machine manages a power level of the receiver processor based on a utilized capacity of the application buffer.

39. (currently amended) The system of claim [[37]] 38, wherein the receiver processor begins in a low power, low clock rate mode.

40. (currently amended) The system of claim [[37]] 38, wherein the receiver processor enters a high power, high clock rate mode when the application buffer reaches a maximum capacity.

41. (currently amended) An article comprising:

a computer-readable storage medium having stored thereon instructions that when executed by a computer result in the following:

receiving a data packet at a receiver protocol state machine, the data packet being transmitted from a transmitter protocol state machine over a data communication

network;

depositing the data packet in an application buffer;

processing and verifying the data packet; and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the receiver protocol state machine manages a power level of a processor in the receiver which is coupled to the receiver protocol state machine based on a utilized capacity of the application buffer, the processor in the receiver switching to a high-power, high clock rate mode from a low power, low clock rate mode when the application buffer reaches a threshold.

Claim 42 (cancelled).

43. (currently amended) ~~The article of claim 42, including instructions, which when executed by the computer result in the processor entering~~

An article comprising:

a computer-readable storage medium having stored thereon instructions that when executed by a computer result in the following:

receiving a data packet at a receiver protocol state machine, the data packet being transmitted from a transmitter protocol state machine over a data communication network;

depositing the data packet in an application buffer;

processing and verifying the data packet; and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the receiver protocol state machine manages a power level of a processor coupled to the receiver protocol state machine based on a utilized

capacity of the application buffer, and a processor in the receiver enters a high power, high clock rate mode when the application buffer reaches a maximum capacity and the processor in the receiver ~~entering~~ enters an idle low power, low clock rate mode after the application buffer has reached the maximum capacity and the receiver protocol state machine has processed packets residing in the application buffer.

44. (previously presented) The article of claim 41, wherein the utilized capacity of the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor in a transmitting device.

45. (previously presented) The article of claim 41, wherein the data communication network includes at least one of the Internet and an Intranet.

46. (currently amended) A receiver for managing energy usage of a processor in the receiver, comprising:

a protocol state machine to receive a packet from a transmitter over a data communication network and to process and verify the packet;

a processor coupled to the protocol state machine; and

an application buffer coupled to the protocol state machine to store the packet,

wherein the protocol state machine transmits an acknowledgment of receipt of the data packet to the transmitter, [[and]] the protocol state machine manages a power level of the processor in the receiver based on a utilized capacity of the application buffer, the processor in the receiver switching to a high-power, high clock rate mode from a low power, low clock rate mode when the application buffer reaches a threshold.

Claim 47 (cancelled).

48. (currently amended) ~~The receiver of claim 46,~~

A receiver for managing energy usage of a processor, comprising:

a protocol state machine to receive a packet from a transmitter over a data communication network and to process and verify the packet;

a processor coupled to the receiver protocol state machine; and

an application buffer coupled to the protocol state machine to store the packet,

wherein the protocol state machine transmits an acknowledgment of receipt of the data packet to the transmitter and the protocol state machine manages a power level of the processor based on a utilized capacity of the application buffer and wherein the processor enters an idle low power, low clock rate mode after the application buffer has reached the maximum capacity and the receiver protocol state machine has processed packets residing in the application buffer.

49. (previously presented) The receiver of claim 46, wherein the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor in a transmitting device.

50. (currently amended) A method of managing energy usage of a processor in a receiver, comprising:

receiving a data packet at a receiver protocol state machine, the data packet being transmitted from a transmitter protocol state machine over a data communication network;

depositing the data packet in an application buffer;

processing and verifying the data packet; and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the receiver protocol state machine manages the a

power level of the processor in the receiver which is [[,]] coupled to the receiver protocol state machine, based on a utilized capacity of the application buffer, the processor in the receiver switching to a high-power, high clock rate mode from a low power, low clock rate mode when the application buffer reaches a threshold.

Claim 51 (cancelled).

52. (currently amended) ~~The method of claim 51,~~

A method of managing energy usage of a processor in a receiver, comprising:

receiving a data packet at a receiver protocol state machine, the data packet being transmitted from a transmitter protocol state machine over a data communication network;

depositing the data packet in an application buffer;

processing and verifying the data packet; and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine, wherein the receiver protocol state machine manages the a power level of the processor based on a utilized capacity of the application buffer, the processor enters a high power, high clock rate mode when the application buffer reaches a maximum capacity, and the processor ~~entering~~ enters an idle low power, low clock rate mode after the application buffer has reached the maximum capacity and the receiver protocol state machine has processed packets residing in the application buffer.

53. (currently amended) The method of claim [[51]] 50, wherein the application buffer and a timer cause periodic patterns in data packet reception, which are used to manage power and frequency of a processor in a transmitting device.

54. (currently amended) The method of claim [[51]] 50, wherein the data communication network includes at least one of the Internet and an Intranet.

Claims 55 – 57 (cancelled).

58. (currently amended) A method of managing energy usage of a processor in a transmitting device, comprising:

invoking a protocol state machine to send a packet across a data communication network to a receiver and waiting for an acknowledgment of receipt;

storing incoming packets that are to transmitted by the protocol state machine to the receiver in a buffer;

managing a power level of the processor in the transmitting device based on a utilized capacity of the buffer;

~~The method of claim 57, wherein the protocol state machine does~~ not ~~transmit~~ transmitting any of the packets in the buffer until the utilized capacity of the buffer reaches the threshold; and

switching the power level of the processor to a low power, low rate clock mode after the packets in the buffer have been transmitted.